REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the final Official Action dated 2 June 2005. Responsive to the rejections made by the Examiner in the Official Action, Claims 1, 5 and 6 have been amended and are now clearer in their respective recitations. Claims 1-10 will be pending in this Application upon entry of the Amendment filed herewith.

In the Official Action, the Examiner rejected Claims 1-3 and 5-7 under 35 U.S.C. § 103(a) as being unpatentable over Fujii, et al. (U.S. Patent #5,898,695; hereinafter Fujii) in view of Aoki, et al. (U.S. Patent #5,771,331). In setting forth the rejections, the Examiner reasserted from the previous Office Action of 2 November 2004 alleged equivalence the packet landing buffer 71 of Fujii with the claimed ring buffer and the claimed error resilience module with contents of program memory 205 recited by Fujii. The Examiner then acknowledged that Fujii does not disclose the claimed access to data in the ring buffer as "by both sequentially increasing memory addresses and sequentially decreasing memory addresses" or "storing the bitstream in a ring buffer subsequently to the video bitstream being inspected for error and prior to correction thereof" or the claimed "means for storing data logging information corresponding to the video bitstream in the ring buffer" and relied on Aoki for the disclosure of such. In applying Aoki, the Examiner referred to, among other examples, Fig. 8 as showing the read pointer RP, allegedly fulfilling the claimed data logging information being stored

in the ring buffer. The Examiner concluded that it would have been obvious to one skilled in the art at the time of the invention of the subject Patent Application to incorporate the ring buffer of Aoki in the buffer circuit of Fujii "to produce a double-speed and increase the capacity of buffer during the video bitstream being decoded. Doing so would allow the video decoder to correct the error while decoding video bitstream".

The Examiner further rejected Claims 4 and 8-10 under 35 U.S.C. § 103(a) as being unpatentable over Fujii in view of Aoki as applied to Claims 1 and 6, and further in view of Kadono (U.S. Patent 6,757,332). The Examiner relied on the teachings of Kadono to show an MPEG-4 compliant decoder in that Fujii teaches only an MPEG decoder. The Examiner concluded that it would have been obvious to one of ordinary skill in the art to incorporate the MPEG-4 compliant decoder of Kadono into the video bitstream decoder of Fujii for the purpose of decoding any video encoded bitstreams.

Applicant's data management systems and methods utilize a ring buffer to store a video bitstream during an error resilient decoding process performed thereon. The data may thereby be read from the video bitstream multiple times, from multiple locations and in multiple directions. Thus, storage of data to the ring buffer is achieved "selectively by one of: accessing sequentially increasing addresses thereof or accessing sequentially decreasing addresses thereof" and retrieval of data is achieved "selectively by one of: sequentially increasing

memory addresses thereof, sequentially decreasing memory addresses thereof or by random access to a specified memory address thereof". The ring buffer may then be coupled to an error resilience module which is used to "select an error correction procedure from a plurality of error correction procedures, the error correction procedure corresponding to an error in the video bitstream stored in the ring buffer as determined by analysis thereof in both a forward direction and a reverse direction". The ring buffer may also be utilized in "storing ... data logging information corresponding to the video bitstream data", where "the data logging information [is] aligned in memory with the corresponding video bitstream data". By the such arrangement, Applicant's invention, "concurrently retriev[es] both a portion of the video bitstream data from the ring buffer and a corresponding portion of the data logging information from the ring buffer responsive to a request for retrieving the portion of the video bitstream data from the ring buffer".

The full combination of these and other features now more clearly recited by Applicant's pending claims is nowhere disclosed by the cited Fujii reference. A careful reading of Fujii clearly reveals the extent to which the teachings thereof rely on the unidirectional access to data in the packet landing buffer described in column 6, lines 14-17, i.e., "the packet landing buffer 71 is a first-in-first-out (FIFO). Only one packet is written in each line in the landing order, **and read in the same order**" (emphasis added). Each time a packet is written to Fujii's packet

landing buffer, an interrupt of the microprocessor is triggered and an indication of the landing time of that packet is also written to the packet landing buffer. The landing time is the value of an up-timer acquired at the time of the interrupt. The write address to the landing buffer is incremented also responsive to the interrupt of the microprocessor. In this way, both the packet landing times and the landing buffer addresses are incremented synchronously. This relationship is essential to Fujii in preventing not only the reading of old data from the buffer (column 7, lines 7 – 9), but also in the recovery of the transport channel clock (column 8, line 34 – column 9, line 9), which is used extensively in the system of the reference. Thus, far from suggesting a buffer in which "the video bitstream [is] stored in selectively either sequentially increasing or sequentially decreasing addresses", as the amended claims of the subject Patent Application now more clearly recite, Fujii **actively teaches away** from such.

Contrary to the Examiner's stated motivation to combine references with Fujii to show obviousness of Applicant's ring buffer, the incorporation into Fujii of **any** bidirectional buffer used in the manner suggested by the Examiner would **change the principle of operation** thereof as illustrated in Fig. 4 and the corresponding description of the Figure in column 6 of the reference. Fujii **teaches away** from any functionality allowing the presently claimed "video bitstream data in the ring buffer being accessible selectively by one of: sequentially increasing memory addresses thereof, sequentially decreasing

memory addresses thereof or by random access to a specified memory address thereof" as **such access would result in catastrophic decoding errors** owing to the unidirectional addressing through which the data are written into Fujii's buffer. And, to necessarily implement in Fujii a buffer by which "the video bitstream [is] stored in selectively either sequentially increasing or sequentially decreasing addresses", a corresponding selectivity in the counting direction of Fujii's up-timer would be required to correctly recover timing information essential to Fujii. Such selectivity is not disclosed, suggested or even alluded to in Fujii and only the **improper application of hindsight** would forward such consideration.

Clearly then, the incorporation of the secondarily cited Aoki into Fujii, as suggested by the Examiner, would require a redesign of Fujii's up-timer to accommodate Aoki's bidirectional buffer. Thus, it is respectfully submitted that **the combination of Fujii and Aoki is improper**, as such would prohibit essential functions of Fujii from being performed. For the same reasons, Fujii may not be combined with **any** bidirectionally addressed buffer of the prior art.

As stated above, Aoki was also cited by the Examiner as showing "means for storing data logging information corresponding to the video bitstream in the ring buffer" and the Examiner referred to Fig. 8 of the reference to illustrate Aoki's capability of such. However, contrary to the Examiner's assertion, Fig. 8 does not show the read pointer RP as being stored in the ring buffer thereof, but rather provides an exemplary location in the ring buffer at which RP could

currently point. Indeed, it would be at a minimum superfluous to store the value of RP at the location in the buffer to which RP is pointing, in that such action constitutes storing the address of the buffer at the address of the buffer. Obviously, such utilization of memory is wasteful and, as such, is atypical of conventional buffer operation. Aoki, rather, uses the ring buffer thereof for exclusively video data storage for the purposes of reconstruction and playback in forward and reverse directions. Nowhere in the reference is there disclosed means for "storing data logging information corresponding to the video bitstream data in the ring buffer, the data logging information being aligned in memory with the corresponding video bitstream data", or means for "select[ing] an error correction procedure from a plurality of error correction procedures, the error correction procedure corresponding to an error in the video bitstream stored in the ring buffer as determined by analysis thereof in both a forward direction and a reverse direction", as does the invention of the subject Patent Application, as now claimed. Thus, it is respectfully submitted that neither Fujii nor Aoki disclose or suggest the beneficial combination of features of Applicant's invention, as now claimed.

Given such contrary teachings of the cited Fujii and Aoki references, the disclosure of the secondarily cited Kadono reference is found to be quite ineffectual to the present patentability analysis. While Kadono does show the use of a MPEG-4 decoder and the related use of video object plane (VOP) data, the

reference does not show, or even suggest, the claimed ring buffer elements and associated method steps now claimed.

All of Applicant's pending independent Claims now recite the limitation of "video bitstream being stored in selectively either sequentially increasing or sequentially decreasing addresses". Claim 1 further recites "select[ing] an error correction procedure from a plurality of error correction procedures, the error correction procedure corresponding to an error in the video bitstream stored in the ring buffer as determined by analysis thereof in both a forward direction and a reverse direction" and independent Claims 5 and 6 further recite "storing in the ring buffer data logging information corresponding to the video bitstream data". It is respectfully submitted that the Fujii, Aoki, and Kadono references, even when properly considered together, fail to disclose the unique combinations of elements and related method steps now more clearly recited by Applicant's pending claims for the purposes and objectives disclosed in the subject Patent Application. Thus, as the amendments to the Claims **merely clarify the recitations of subject matter already considered by the Examiner**, it is now believed that the independent Claims of the subject Patent Application are in condition for allowance. Additionally, it is further believed that the dependent Claims are allowable for **at least** the same reasons for which the independent Claims on which they are based are allowable.

The remaining Patents cited by the Examiner but not used in the rejections have been reviewed, but are believed to be further remote from the subject Patent Application than the references used by the Examiner when patentable considerations are taken into account.

In view of the foregoing amendments and remarks, Applicant believes that the subject Patent Application is in condition for allowance and such action is respectfully requested.

Respectfully submitted,
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